AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

Kindly cancel claims 1-9 without prejudice or disclaimer.

Kindly add new claims 10-17 as follows.

10. (New) A method of allocating functionality to processor elements in a processor array, wherein the processor array comprises a plurality of processor elements arranged in an array of rows and columns, the processor elements being interconnected by buses running between the rows and columns and by switches located at the intersections of the buses, wherein, in operation of said processor array, data is transferred during time slots between processor elements over horizontal buses running between the rows of processor elements and over vertical buses running between the columns of processor elements, the method comprising:

identifying one row as a redundant row to which no functionality is initially allocated, such that, in the event that a first processor element is found to be faulty, functionality can be removed from the row that contains said first processing element, and can be allocated instead to the redundant row; and

when allocating functionality to the processor elements, such that data is scheduled to be transferred during a first time slot from a first processor element in a first row to a second processor element in a second row, which is different from the first row, via one of said switches without using any vertical bus, reserving said time slot for said scheduled data transfer on a segment of a vertical bus that would be used in the event of a reallocation of functionality following a determination that either said first processor element or said second processor element was faulty.

11. (New) A method as claimed in claim 10, further comprising:

in the event that a first processor element is found to be faulty, allocating the functionality, removed from the row that contains said first processing element, to an adjacent row; and reallocating the functionality from the adjacent row, to a further row adjacent thereto, as required until functionality has been allocated to the redundant row.

12. (New) A method as claimed in claim 10, wherein the redundant row is located at an edge of the array.

13. (New) A method as claimed in claim 11, wherein the redundant row is located at an edge of the array.

14. (New) A processor array, comprising:

a plurality of processor elements arranged in an array of rows and columns; buses running between the rows and columns; and

switches located at the intersections of the buses, wherein the processor elements are interconnected by the buses and the switches,

wherein the processor array is adapted to transfer data during time slots between processor elements over horizontal buses running between the rows of processor elements and over vertical buses running between the columns of processor elements,

wherein one row is identified as a redundant row to which no functionality is initially allocated, such that, in the event that a first processor element is found to be faulty, functionality can be removed from the row that contains said first processing element, and can be allocated instead to the redundant row; and

wherein, when allocating functionality to the processor elements, such that data is scheduled to be transferred during a first time slot from a first processor element in a first row to a second processor element in a second row, which is different from the first row, via one of said switches without using any vertical bus, the processor array is adapted to reserve said time slot for said scheduled data transfer on a segment of a vertical bus that would be used in the event of a reallocation of functionality following a

determination that either said first processor element or said second processor element was faulty.

15. (New) A processor array as claimed in claim 14, wherein the arrangement of processor elements in each row is the same as the arrangements of processor elements in each other row, wherein said horizontal buses comprise pairs of horizontal buses running between the rows of processor elements, each pair comprising a first horizontal bus carrying data in a first direction and a second horizontal bus carrying data in a second direction opposite to the first direction, wherein some pairs of adjacent columns of processor elements have no vertical buses running therebetween, and other pairs of adjacent columns have two buses carrying data in a first direction and two buses carrying data in a second direction opposite to the first direction running therebetween, and wherein said switches are located at the intersections of the horizontal and vertical buses.

16. (New) A processor array as claimed in claim 15, wherein each switch comprises:

a plurality of input buses and a plurality of output buses;

a memory device, which stores information at each address thereof, indicating what data is to be switched onto each of the output buses; and

a controller, for counting through addresses of the memory device in a predetermined sequence.

17. (New) A processor array as claimed in claim 16, wherein the memory device stores information which indicates whether the data to be switched onto each of the output buses is:

the data value on one of the input buses;

the previous data value on said output bus; or

the value zero.